## **REMARKS**

Claims 1-2, 7-12, and 33-40 are pending in this application, claims 41 to 56 having been withdrawn from consideration as being directed to a non-elected invention. The Examiner has maintained the following section 103 obviousness rejections:

Claims 1, 7-9, and 11-12 over U.S. Patent No. 5,920,084 (<u>Gu</u>, et al.) in view of U.S. Patent No. 5,053,844 (<u>Murakami</u>, et al.);

Claims 33, 37, and 39-40 over <u>Gu</u> in view of U.S. Patent No. 5,646,756 (<u>Dohjo</u>, et al.) and U.S. Patent No. 5,668,379 (<u>Ono</u>, et al.);

Claims 2 and 34-36 over Gu, Murakami, Dohjo, and Ono;

and

Claims 10 and 38 over <u>Gu</u>, <u>Murakami</u> and <u>Dohjo</u>, <u>Ono</u>, and further in view of U.S. Patent No. 5,671,027 (<u>Sasano</u>, et al.).

With regard to claim 1, in the Final Office Action, the Examiner alleges that recognizing another advantage that would flow from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. In particular, the Examiner states that "[s]imply because Applicant has recognized that one purpose of the a-Si:O:F insulating layer is to reduce or minimize parasitic capacitance does not preclude such use of the insulating layer from advantages associated with reducing the band gap thickness...."

Applicant respectfully disagrees.

Applicant urges that there is no motivation or suggestion to combine an a-Si:O:F of Gu and thin film transistor panel of Murakami according to the teaching of Gu. The Examiner's argument that recognizing the utility of an a-Si:O:F insulating layer to reduce parasitic capacitance does not preclude its use in reducing band gap thickness is irrelevant, since the issue is whether using a a-Si:O:F layer to reduce bad gap renders obvious its use to reduce capacitance. Applicant urges that the advantages associated with reducing the band gap in a photo-sensor do not motivate applying an a-Si:O:F layer as a passivation layer of a thin film transistor array panel since reducing the band gap in a photo-sensor does not provide any advantage or effect for a passivation layer in a thin film transistor array panel. Applicant is not urging that patentability be admitted because Applicant has recognized another advantage of a-Si:O:F, but rather that there is no motivation to combine a-Si:O:F of Murakami's photo-sensor with a thin film transistor panel according the description of Gu.

Therefore, Applicant urges that claim 1 is not *prima facie* obvious in view of <u>Gu</u> and Murakami. Reconsideration and withdraw of this rejection are respectfully requested.

Claims 2 and 7-12 depend from claim 1, and are thus patentable for at least the same reasons as claim 1. Reconsideration and withdraw of these rejections are respectfully requested.

With regard to claim 33, the Examiner argues that "nowhere in the claim does it specify that the bottom layer [of the first insulating layer] must be an insulating layer."

Applicant respectfully disagrees.

Applicant urges that by reciting that "the first insulating layer includes a top layer and a bottom layer", the claim is specifying that the bottom layer is an insulating layer. Furthermore, Applicant does not agree with the Examiner's statement that "even a semiconductor layer can function to 'insulate' one portion of the array with another", as by that interpretation any layer in a TFT array can serve that purpose. However, a semi-conductor layer will not in general serve to electrically insulate one layer from another, and does not serve that purpose in <u>Dohjo</u>, since <u>Dohjo</u> specifically discloses insulating layers 14 and 15 that serve that purpose. Thus, Applicant urges that <u>Dohjo</u> does not disclose or suggest a first insulating layer includes a top layer and a bottom layer, the bottom layer being an a-Si:O:F layer, and the top layer being a silicon nitride layer, as recited in claim 33.

Applicant has amended claim 33 to recite "the bottom layer being an a-Si:O:F layer", a feature previously recited in claim 34. The Examiner has cited <u>Ono</u> for disclosing a substrate with a dielectric constant about 4 or less. However, the passage of <u>Ono</u> cited by the Examiner discloses either an SiO<sub>2</sub> film, or a film made of two layers of SiO<sub>2</sub> and SiN. <u>Ono</u> does not disclose or suggest a film having a *bottom layer being an a-Si:O:F layer*.

Thus, Applicant urges that the combination of <u>Gu</u>, <u>Dohjo</u>, and <u>Ono</u> do not teach or suggest all of the claimed features of claim 33. Therefore, Applicant urges that a *prima facie* case of obviousness of claim 33 over the combination of <u>Gu</u>, <u>Dohjo</u>, and <u>Ono</u> cannot be maintained. Reconsideration and withdraw of these rejections are respectfully requested.

Claims 35-40 depend from claim 33, and are thus patentable for at least the same

reasons as claim 33. Reconsideration and withdraw of these rejections are respectfully requested.

## **CONCLUSION**

Applicant urges that claims 1-2, 7-12, 33, and 35-40 are in condition for allowance for at least the reasons stated. Early and favorable action on this case is respectfully requested.

Respectfully submitted,

By:

David L. Heath Reg. No. 46,763

Attorney for Applicant

## **Mailing Address:**

F. Chau & Associates, LLC 130 Woodbury Road Woodbury, NY 11797 (516) 692-8888 (516) 692-8889 (FAX)